Ramsey Z. Doany

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EDUCATION

Texas State University — San Marcos, Texas
MS Electrical Engineering (**GPA: 4.0**) — May 2018

Texas State University — San Marcos, Texas
BS Electrical Engineering — May 2016

PUBLICATIONS

Early Collision Detection and Handling in CDMA-based RFID Systems — Feb 2018
Provisional Patent Application

A CDMA-based RFID Inventory System — May 2016
IEEE International Conference on RFID 2016

EXPERIENCE

Southwest Research Institute — San Antonio, Texas
Engineer - Space Science & Engineering Division — Jan 2018 - Present

- Lead FPGA Engineer, designed, wrote, tested, and implemented flight-destined Verilog and VHDL to enable command communication and routing within the satellite itself and between the satellite and the Earth
- Lead FPGA Engineer, designed ground support equipment to debug and test flight-destined hardware using LabVIEW FPGA and LabWindows. This also involved analog and mixed-signal circuit design
- Researcher, reviewed and characterized performance of image tracking algorithm for object tracking telescope system using MATLAB
- Researcher, designed, wrote, and tested Verilog for use in development of high speed processing module for in-flight data processing and communication
- Generated presentations, visualizations, and reports for customer-involved design reviews and acted as Assisted Project Manager in said design reviews

Texas State University — San Marcos, Texas
Graduate Research Assistant — Aug 2016 - Jan 2018

- Designed and simulated novel UHF RFID MAC protocols using Verilog and MATLAB
- Wrote reports and presented on RFID, real-time speech compression techniques, and software defined radio

Emerson Process Management — Austin, Texas
Hardware Engineering Intern — May 2014 - Aug 2014

- Designed and built perfboard and breadboard based test circuits for control system hardware

- Debugged and wrote reports on malfunctioning control system equipment

SKILLS

- Proficient in Verilog, Labview FPGA, and FPGA implementation for processor and SoC design
- Certified Labview Associate Developer (CLAD)
- Proficient in analog circuit design and electronics including the use of high frequency components such as oscillators and phase-locked loops
- Proficient in the use of information theory for data compression and error control coding for communication systems
- Expertise in communication theory including modulation schemes, transmitter/receiver design, and multiplexing/media access schemes with particular expertise in UHF RFID protocols, and tag & interrogator architecture and design
- Knowledge in wireless and cellular communication networks
- Expertise in circuit design and modeling using LTSpice and Multisim
- Proficient in using MATLAB and Simulink for mathematical simulation, communication system modeling, and digital signal processing
- Experience using Arduino, Raspberry Pi, and NI MyRIO, Python, C/C++, and R

UNIVERSITY AWARDS

Ingram School of Engineering Director's List 2017 & 2018

Graduate College Research Support Fellowship - Grant 2017

PROJECTS

Design of a Novel Medium Access Control Protocol for Optimization of CDMA-based Passive RFID: Bitwise CDMA- *MS Thesis*

Jan 2017 - Present

- Designing a passive UHF RFID MAC protocol optimized for CDMA multiplexing using Verilog and LabVIEW
- A provisional patent application has been filed based on this work

FPGA Implementation of a Walsh Code Encryption Algorithm

March 2017

- Designed a cryptographically secure pseudorandom encryption algorithm using Walsh-Hadamard sequences that encrypts, scrambles, and compresses an incoming bitstream
- Tested algorithm using MATLAB, wrote algorithm in Verilog and implemented it on an FPGA

CDMA-based RFID Inventory System - *Undergraduate Senior Design Project*

Jan 2015 - Dec 2015

- Designed and created software simulation of proposed system in MATLAB
- Designed and built hardware simulation of proposed system using an arbitrary waveform generator, MATLAB, software defined radio, and GNURadio
- Published paper and presented results at IEEE International Conference on RFID 2016