Ingram School of Engineering, Texas State University

EE 4355, Analog and Mixed Signal Design

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Phase-Locked Loop FSK Demodulator

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Statement of Problem

Phase-Locked Loops are an incredibly powerful tool in electronics design. PLLs can be used in many applications including frequency synthesization, FSK demodulation, and PSK demodulation. This laboratory is designed to familiarize students with the properties and use of PLL circuits by having the students design and construct a PLL FSK demodulator. FSK stands for Frequency Shift Keying and is a key concept in digital communication as a whole and in particular is extremely important in FM (frequency modulation) systems. FSK modulation takes a binary stream and converts it into an analog signal to be transmitted over some medium. The simplest form of binary shift keying requires a carrier frequency, f_c and 2 frequencies, equidistant in Hz (Δf) from the carrier frequency to represent either a binary "1" or a binary "0". Generally, $f_c + \Delta f$ represents "high" or "1" and $f_c - \Delta f$ represents "low" or "0". These frequencies are referred to as f_H and f_L, respectively. An FSK demodulator receives a modulated signal whose frequency changes between f_H and f_L and outputs a "high" DC voltage level or "low" DC voltage level to indicate that the bit transmitted at that point in the bitstream was either a 0 or a 1. For this specific laboratory exercise, the output is to be TTL-compatible, meaning that the output of the demodulator should either be a positive DC voltage or 0 volts.

Specifications

Minimum Input Signal	500mV
Input MARK (HI) Frequency	1.025kHz
Input SPACE (LO) Frequency	0.975kHz

Maximum Baud Rate	100Hz
Minimum Baud Rate	0Hz
S/N ratio	20dB
Output	TTL-compatible

Table 1. Required specifications of Phase-Locked Loop Frequency Shift Keying Demodulator.

Design Approach and Description

The first step in designing the PLL FSK demodulator was to determine the block diagram for how the system is to function. This basic block diagram consists of an amplification stage, a PLL stage, and a comparator stage.

1. The Amplification Stage

Rather than designing an inverting or noninverting amplifier, A simple op-amp comparator was used. This decision was made based on the fact that, since the input of the op-amp was a square wave and the output was to be a square wave as well, the input voltage of the op-amp could simply be compared to the average voltage level of the incoming signal and the output of the op-amp would hit the positive and negative rails, giving maximum amplification and having the same square wave amplitude level entering the input of the PLL, no matter the signal level.

2. The PLL Stage

The CD4046BE CMOS PLL IC was the PLL chip used in this design. The CD4046D IC has two main sections for monitoring phase locking: The output of an XOR block that

exclusive-ors the local oscillator of the PLL and the input signal and the output of a charge pump that outputs pulses the width of which indicate the phase difference between the local oscillator of the PLL and the input signal. The output of the XOR was used in this design. The first input block of the system was selected to be an amplifier to meet the minimum signal amplitude requirement.

Next, using equations 1, 2, and 3, component values were selected so that the VCO frequency was a value such that the PLL could reliably lock on to the carrier frequency, the "high" frequency, and the "low frequency" and the cutoff frequency of the loop amp was such that the output signal would have relatively little noise while meeting the 100Hz baud rate specification. In the mentioned equations, K_c is the VCO constant, V_9 is the DC voltage at pin 9 of the PLL chip, ω is the local oscillator frequency, f_{co} is the cutoff frequency of the loop filter, and R_{VCO}, C_{VCO}, R, and C are R5, C3, R4, and C1 on the circuit diagram in Figure 1, respectively.

$$K_c = (8.8)\left(\frac{1}{R_{VCO}C_{VCO}}\right)^{0.8} \quad \textbf{(1)}$$

$$\omega = K_c(V_9 - 1) \quad \textbf{(2)}$$

$$f_{co} = \frac{1}{2\pi RC} \quad \textbf{(3)}$$

Depending on the external frequency sent to the XOR part of the chip, the DC voltage level at the VCO input will change. Rather than loading the VCO pin of the PLL chip, the pin connected to the output of the source follower section of the chip was used as it represents the

same DC voltage change and using it will not affect the performance of the PLL since its output is isolated from the rest of the internal circuitry of the PLL.

3. The Comparator Stage

The final stage of the FSK demodulator is the comparator stage. The comparator utilizes the output of the source follower of the PLL. When the input of the PLL is the frequency representing a binary “0”, the source follower outputs a positive DC voltage with a slight ripple and when the input of the PLL is the binary “high” frequency, the output of the source follower is a slightly higher DC voltage with a slight ripple. To aid in avoiding errors, a low-pass filter was added to remove the ripple as best as possible. The output of this low-pass filter was then connected to a TS372CN comparator chip to be compared to the mean DC voltage level between the source follower output when the input of the circuit is the “high” frequency and when the input is the “low” frequency. With the rails of this comparator set to 5V and ground with resistors put in place to set the voltage to which the input is to be compared to, the TTL-compatible demodulated output of the system was taken from the output of the comparator. To prevent unwanted noise from the power supply, a bypass capacitor was placed across the rails of the comparator.

The full circuit that was designed and constructed in Figure 1 below.

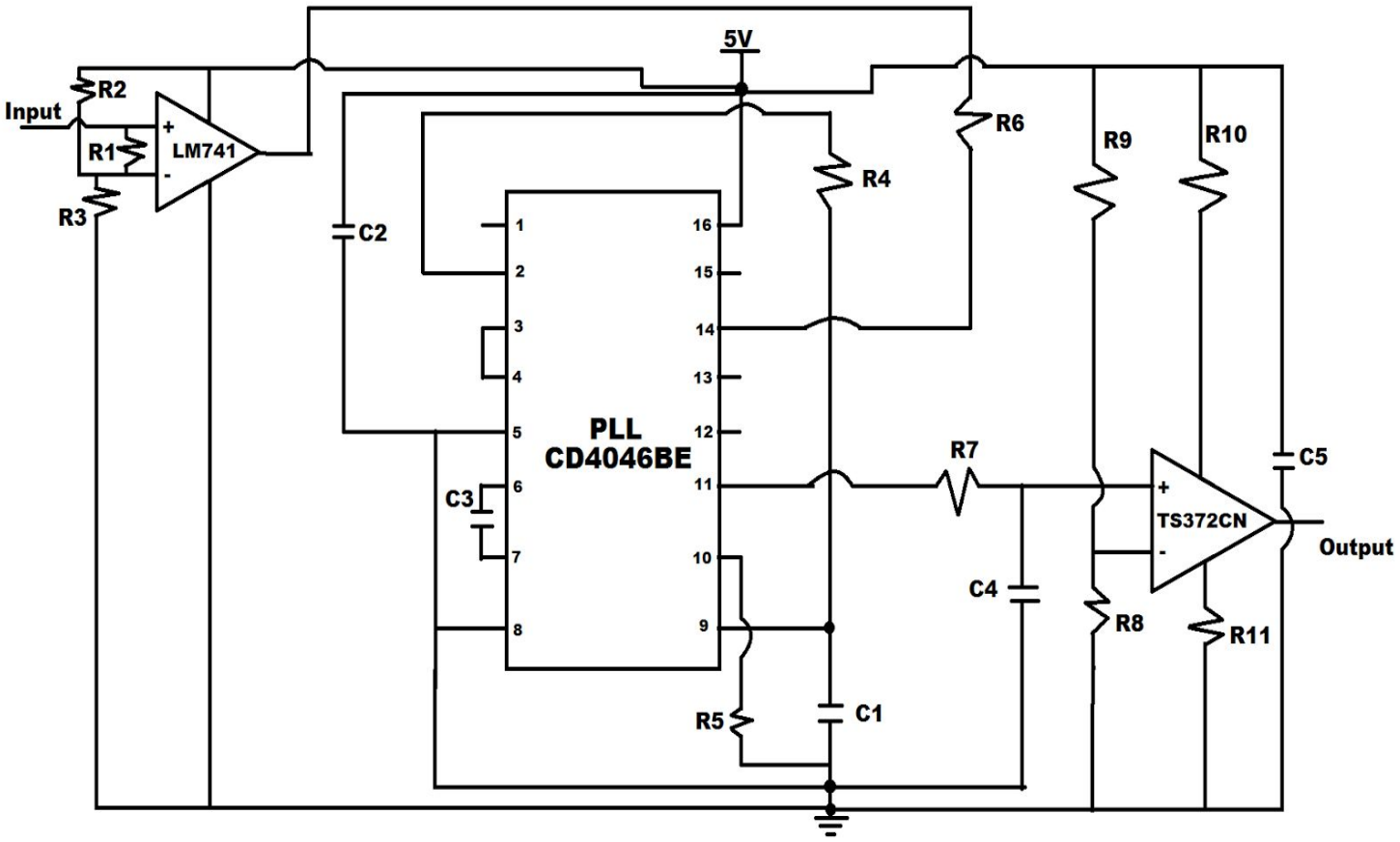

Figure 1. PLL FSK demodulator circuit using the LM741 IC for the amplification stage, the CD4046BE IC for the PLL stage, and the TS372 IC for the comparator stage.

The component values used in the circuit in Figure 1 are listed in Table 2 below:

R1	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R8**
100k Ω	3k Ω	1k Ω	100k Ω	100k Ω	1k Ω	15k Ω	1k Ω
R9	**R10**	**R11**	**C1**	**C2**	**C3**	**C4**	**C5**
7.9k Ω	10k Ω	430 Ω	66nF	1 µF	4.4nF	100nF	1 µF

Modeling and Simulation

While no simulation was done to test this circuit, each separate section was designed, built, and tested before being put together into a full FSK demodulating system. In doing so, a lot of discussion and pen-and-paper modeling of how the system would work was done, including the method of amplification and the TTL output of the comparator.

Experimental Results

To test the functionality of the circuit, a function generator with modulation capabilities was used to generate the FSK waveform sent through the system for demodulation. Since the control voltage for the system was 5V, the input signal was given a 2.5V DC offset to give the signal maximum "swing" between the rails of the circuit. The input and output of the circuit were connected to channel 1 and channel 2 of an oscilloscope to observe whether or not the circuit was functioning properly. The modulated input and demodulated output of the circuit can be seen in Figure 2 below.

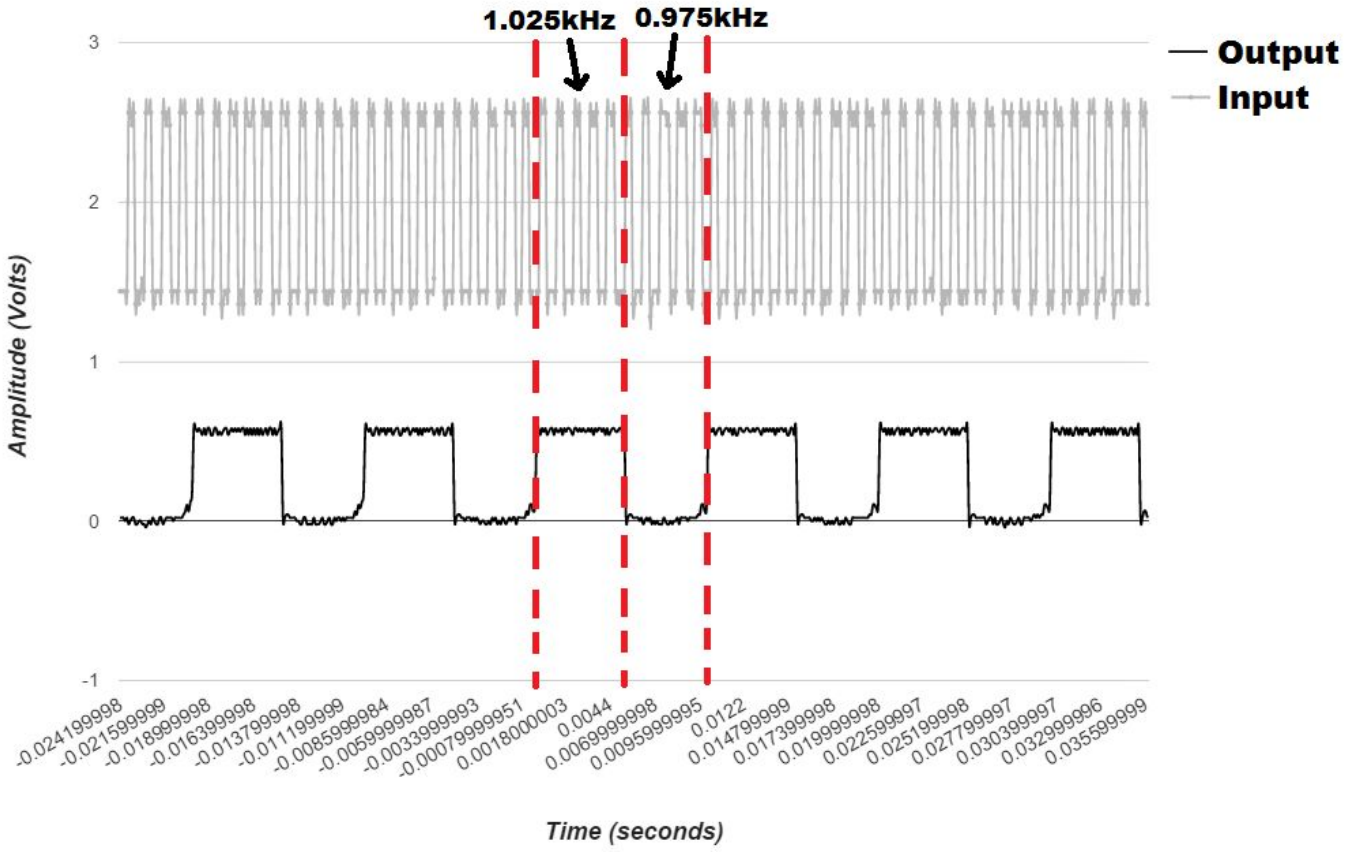

Figure 2. Oscilloscope plot of input and output of FSK demodulator circuit showing TTL-compatible output switching between MARK and SPACE depending on input frequency. Some bit periods are highlighted to show how the output changes depending on input frequency.

The system was tested with a variety of input amplitudes ranging from 500mV to 5V and baud rates ranging from 1Hz to 200kHz and passed under these conditions. The signal-to-noise ratio of this system was determined by comparing the RMS voltage value of the output with an input signal present to the RMS voltage value of the output with no input present.

Performance Summary

The laboratory exercise was a success. The performance of the circuit met all of the required specifications. A comparison of the required specifications and the actual performance of the circuit can be seen in Table 3 below.

Parameter	**Requirement**	**Actual Circuit Performance**
Minimum Input Signal	500mV	500mV
Input MARK (HI) Frequency	1.025kHz	1.025kHz
Input SPACE (LO) Frequency	0.975kHz	0.975kHz
Maximum Baud Rate	100Hz	200Hz
Minimum Baud Rate	0Hz	0Hz
S/N ratio	20dB	25.7dB
Output	TTL-compatible	TTL-compatible

Table 3. Comparison of circuit performance requirements and actual circuit performance.

Bill of Materials

-LM741 Operational Amplifier

-CD4046BE Phase-Locked Loop

-TS372CN Comparator

-Resistors

- 3 x 100kΩ
- 3kΩ
- 2 x 1kΩ
- 15kΩ
- 7.9kΩ
- 10kΩ
- 430Ω

-Capacitors

- 66nF
- 2 x 1μF
- 4.4nF
- 100nF